

# Themis TPA-XMC High-Performance Low-Power PrXMC Computer

## Uses the new P.A. Semi PWRficient<sup>™</sup> Platform Processor

**Product Brief** 

The TPA-XMC expands the Themis 64-Bit PowerPC Embedded Computer product line with a PrPMC/PrXMC card based on the P.A. Semi PA6T-1682M PWRficient Platform Processor. The TPA-XMC is a single-wide card configured with a 2.0GHz Dual 64-bit enhanced Power Architecture<sup>™</sup> processor. This new P.A. Semi Platform Processor is Power Architecture compatible, and runs new or existing 32 or 64-bit PowerPC code. This new device also features VMX (AltiVec<sup>™</sup> compatible) SIMD Vector Processing Units and features industry leading processing performance per watt. This board can auto-sense and operate in both Monarch or non-Monarch mode. Eighteen user-configurable SERDES lanes are available to serve a wide range of high-speed I/O requirements. Serdes I/O options include Gigabit and 10 Gigabit Ethernet and PCI-Express. There is support for both convection (air) and conduction cooled options. The Themis TPA-XMC provides powerful dual 64-bit superscalar SMP RISC processing, flexible high-speed I/O, and low power consumption in a small, rugged form factor.

#### **TPA-XMC Features and Specifications:**

- P.A. Semi PA6T-1682M Dual Core 2.0GHz Processor
- Dual Port 2MByte Shared L2 Cache
- DDR2 Memory Controller
- Built-In Computation and Transformation Offload Engines for:
  - Bulk Encryption
  - Cyclic Redundancy Checking (CRC)
  - Streaming XOR Generation
- Two 10GB and Four SGMII Protocol Engines Provide:
- Packet Processing, including Line-Rate Packet Filtering
  VLAN Flow Control
  - TCP/IP Acceleration
- Est. Maximum Power: 25 Watts, Est. Typical Power: 15 Watts
- 1 or 2GBytes of DDR2-400 ECC SDRAM Memory (soldered)
- 128Mbytes of OS Kernel NAND Flash Memory
- Real Time Clock with 256 Bytes NVRAM
- 64-bit / 133MHz PCI-X

#### Operating System Support

- Supports Yellow Dog<sup>™</sup> v5.0 64-bit SMP Linux®, VxWorks®
- Boot from network

#### **Operational**

Auto detects Monarch or non-Monarch mode

• Configurable SERDES lanes (18) on XMC connectors

#### P.A. Semi PA6T-1682M PWR ficient Platform Processor Key Architectural Features:

#### 64-bit Superscalar RISC Performance

The P.A. Semi PA6T-1682M RISC Processor – which combines two 2GHz enhanced Power Architecture CPU Cores, two DDR2 memory controllers, 2MB of L2 cache, and a flexible I/O subsystem – is a versatile building block for high performance computing and embedded applications. PWRficient provides industry-leading performance per watt for multi-gigahertz computational applications and multi-gigabit throughput applications. This is the result of a ground-up design that optimizes power dissipation in all aspects of its novel system architecture which comprises an entire platform on a chip.

#### **CONEXIUM™** Coherent Crossbar

The CONEXIUM coherent crossbar is an on-chip fabric that interconnects the two 64-bit superscalar CPUs, two DDR2 memory controllers, a dual-ported 2MB L2 cache, and the ENVOI™ I/O subsystem to deliver on-chip symmetric multiprocessing with coherent I/O.

#### ENVOI™ I/O Subsystem

The ENVOI I/O subsystem provides 24 configurable SERDES lanes for high-speed serial I/O, which may be used for PCI-Express, XAUI, or SGMII interfacing in a wide range of configurations.



| Qty. | Access                                |
|------|---------------------------------------|
| 2    | Front Panel                           |
| 1    | Front Panel                           |
| 9    | XMC Primary Connector                 |
| 9    | XMC Secondary Connector               |
| 64   | PMC I/O Connectors                    |
|      | <b>Qty.</b><br>2<br>1<br>9<br>9<br>64 |

#### Environmental

| Parameter         | Operating                  | Non-Operating |
|-------------------|----------------------------|---------------|
| Temperature Range | 0°C to 50°C (convection)   | -40°C to 95°C |
|                   | -40°C to 85°C (conduction) | -40°C to 95°C |
| Humidity          | 10% to 95%                 | 10% to 95%    |
| (non-condensing)  |                            |               |
| Shock             | 30G @ 40mS                 | 30G @ 40mS    |
| Vibration         | 0.90G (rms)                | 2.97G (rms)   |

# Themis TPA-XMC Block Diagram



### Primary XMC Connector:

| Quad   | Lane(s) | Functions    |
|--------|---------|--------------|
| Quad 2 | 8 - 11  | PCI-e, SGMII |
| Quad 3 | 12 - 15 | PCI-e, XAUI  |
| Quad 5 | 23      | PCI-e, SGMII |

### Secondary XMC Connector:

| Quad   | Lane(s) | Functions    |
|--------|---------|--------------|
| Quad 0 | 0 - 3   | PCI-e        |
| Quad 1 | 4 - 7   | PCI-e        |
| Quad 5 | 22      | PCI-e, SGMII |
|        |         |              |

\* Convection Cooled Version Only



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